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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,067	03/16/2004	Jon M. Huppenthal	ARB001 CON/CIP	3775

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

3/4

Office Action Summary	Application No.	Applicant(s)	
	10/802,067	HUPPENTHAL ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *41-44,46 and 48-50* is/are allowed.

6)☒ Claim(s) *1-40,51,52,55-57 and 60* is/are rejected.

7)☒ Claim(s) *24,25,34,35,37,45,47,53,54,58 and 59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities: US Patent number for US Application 10/452,113 is missing in the first paragraph. Appropriate correction is required.

Claim Objections

Claims 45 and 47 are objected to because of the following informalities: Claim 45, lines 4-5 and Claim 47, line 3, the recitation, "can be" should be changed to "is" in order to particularly point out and distinctly claim the subject matter.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 51 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 51, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23, 26-33, 36, 38-40, 51, 52, 56, 57, and 60 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin (US 6,451,626 B1).

Regarding claim 1, Lin discloses, in Figs. 1A-24, a processor module comprising:

at least first integrated circuit functional element (see 202 in Fig. 7) including a programmable array (col. 14, lines 18+); and

at least second integrated circuit functional element (204 in Fig. 7) stacked with and electrically coupled (via 116, 124, 128, 138, etc.; see col. 4, lines 7+) said programmable array said first integrated circuit functional element.

Regarding claim 2, Lin discloses, in Figs. 1A-24, that wherein said programmable array of said first integrated circuit functional element comprises an FPGA (col. 14, lines 18+).

Regarding claim 3, Lin discloses, in Figs. 1A-24, that wherein said processor of said second integrated circuit functional element comprises a microprocessor (col. 14, lines 18+).

Regarding claim 4, Lin discloses, in Figs. 1A-24, that wherein said second integrated circuit functional element comprises a memory (or memory array; see col. 14, lines 18+).

Regarding claim 5, Lin discloses, in Figs. 1A-24, at least third integrated circuit functional element (268 in Fig. 7) stacked with and electrically coupled (via 124, 128, 138, etc.) to at least one of said first or second integrated functional elements.

Regarding claim 6, Lin discloses, in Figs. 1A-24, that wherein said third integrated circuit functional element comprises a memory (or memory array; see col. 14, lines 18+).

Regarding claim 7, Lin discloses, in Figs. 1A-24, that wherein said programmable array reconfigurable as a processing element (reconfigurable FPGA is intended to be used for the package, see col. 14, lines 18+; it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987)).

Regarding claim 8, Lin discloses, in Figs. 1A-24, that wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points (124) distributed throughout the surfaces of said functional elements.

Claims 9-23 are essentially the same in scope as claims 1-8 and are rejected similarly.

Regarding claim 9, the recitation, "a processor and a memory" is inherent in a computer system.

Regarding claim 26, Lin discloses, in Figs. 1A-24, wherein said memory array is functional as block memory for said processing element (memory array is intended to be used as block memory for the processing element in the stacked package, see col. 14, lines 18+; it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987)).

Regarding claim 27, Lin discloses, in Figs. 1A-24, a reconfigurable processor module comprising:

at least a first integrated circuit functional element (see 202 in Fig. 7) including a programmable array (col. 14, lines 18+);

at least second integrated circuit functional element (see 204 in Fig. 7) including a processor (col. 14, lines 18+) stacked with and electrically coupled to said programmable array of said first integrated circuit functional element; and

at least third integrated circuit functional element (see 268 in Fig. 7) including a memory (col. 14, lines 18+) stacked with and electrically coupled to said programmable array and said processor of said first and second integrated circuit functional elements respectively

whereby said processor and said programmable array are operational to share data (via 116, 124, 128, 138, etc.; see col. 4, lines 7+) therebetween.

Regarding claim 28, Lin discloses, in Figs. 1A-24, that wherein said memory is operational to at least temporarily store said data (DRAMs will inherently store data temporarily; see col. 14, lines 18+).

Regarding claim 29, Lin discloses, in Figs. 1A-24, that wherein said programmable array of said first integrated circuit functional element comprises an FPGA (col. 14, lines 18+).

Regarding claim 30, Lin discloses, in Figs. 1A-24, that wherein said processor of said second integrated circuit functional element comprises a microprocessor (col. 14, lines 18+).

Regarding claim 31, Lin discloses, in Figs. 1A-24, that wherein said memory of said third integrated circuit functional element comprises a memory array (col. 14, lines 18+).

Claims 32, 33, 36, and 38-40 are essentially the same in scope as claims 1-23, 26, 27, and 29-31 and are rejected similarly.

Regarding claim 51, Lin discloses, in Figs. 1A-24, a method of fabricating a processor module comprising:

forming at least a first integrated circuit functional element (see 202 in Fig. 7) including a microprocessor (col. 14, lines 18+) on a base wafer (col. 7, lines 13+); and

using wafer processing techniques (col. 7, lines 13+), forming at least a second integrated circuit functional element (see 204 in Fig. 7) including a field programmable gate array (col. 14, lines 18+) on the first integrated circuit functional element.

Regarding claim 52, Lin discloses, in Figs. 1A-24, forming an electrical contact (124, 128, 138, etc.; see col. 4, lines 7+) between at least one of a plurality of metal pads (116) associated with the first integrated circuit functional element and at least one of a plurality of metal pads associated with the second integrated circuit functional element.

Regarding claim 56, Lin discloses, in Figs. 1A-24, comprising etching through (see 116A) the second integrated circuit functional element so that an electrical interconnection (116, 124, 128, 138, etc.; see col. 1, lines 15+; col. 4, lines 7+) can be established between the first and second integrated circuit functional elements.

Regarding claim 57, Lin discloses, in Figs. 1A-24, comprising forming a third functional element (see 268 in Fig. 7) integrated with the first two functional elements using wafer processing techniques (col. 7, lines 13+).

Regarding claim 60, Lin discloses, in Figs. 1A-24, forming the third functional element comprises forming an I/O controller, memory, FPGA, or microprocessor (col. 14, lines 18+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin.

As applied previously, Lin teaches all the features of the claimed invention, with the exception of teaching the claimed forming a silicon dioxide layer on a top surface of the first integrated circuit functional element. Instead, Lin teaches passivation layer on a top surface of the first integrated circuit functional element.

However, it is well known in the art that a silicon dioxide is used for passivation purpose. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the top surface of the first integrated circuit functional element layer of Lin with the silicon dioxide as passivation layer for passivation purpose.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-40 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7, 9-15, 17-21, 23-30, and 33-38 of U.S. Patent No. 6,627,985 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present application presents claims that are slightly broader versions of the patented claims.

Allowable Subject Matter

Claims 41-44, 46, and 48-50 are allowed.

Claims 45 and 47 would be allowable if the claim objections are corrected.

Claims 24, 25, 34, 35, 37, 53, 54, 58, and 59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and file a terminal disclaimer as stated above.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Lin, taken alone or in combination of other references, does not teach or fairly suggest a method or a module comprising, among other things, that wherein said memory array functional to accelerate reconfiguration of said field programmable gate array as a processing element (claims 24, 34); wherein said memory array is functional to accelerate

external memory references to said processing element (claims 25, 35); wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit functional element (claim 37); forming a first epitaxial layer over the first integrated circuit functional element; and forming at least a second integrated circuit functional element including a memory array in the first epitaxial layer (claim 41); wherein forming the second or third integrated circuit functional element comprises forming an epitaxial layer (claims 53, 58), as set forth in the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Corisis et al. (US 6,072,233) discloses stackable ball grid array package.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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